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B. Tech. EXAMINATION, 2022

(Third Semester)

(C Scheme) (Main & Re-appear)

(CSE, ECE)

ECE203C

DIGITAL SYSTEM DESIGN

Time : 3 *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all. All questions carry equal marks.

1. (a) Draw and simplify a circuit to realize the function :

$$Y = \overline{\overline{A} + \overline{B} + \overline{C}}$$

(b) Simplify using K-map and implement using NAND/NOR gate :

$Y(A, B, C, D) = \Pi M (1, 3, 5, 7, 9, 10, 13, 14)$

2. (a) Differentiate between ROM implementation and RAM implementation.

(b) Explain keyboard encoder and decoder.

3. (a) Realize using 16 : 1 MUX :

$f(A, B, C, D) = \sum m(0, 1, 3, 4, 6, 8, 10, 12, 15)$

(b) Convert in :

(i) $(90)_{10}$ = (BCD)

(ii) $(110101)_2$ = (Octal)

(iii) $(574)_{10}$ = (Octal)

(iv) $(BCA3)_{16}$ = Binary

(v) $(10110)_2$ = (Gray)

4. (a) Design synchronous counter using T flip-flop. Also design mod-8 synchronous up-down counter using T-flip flop.

(b) Explain Moore machine and Mealy machine.

5. (a) Design universal shift register and also explain the working of 8-bit universal shift register with the help of its circuit diagram and truth table.

(b) Realize XNOR function using OR logic.

6. (a) Define the working of two i/p TTL logic NAND gate. Also draw its circuit diagram.

(b) Compare CPLD *vs.* FPGA.

7. (a) Design the building block of SR and T flip-flop.

(b) Define VEM technique with example.

8. Write short notes on the following :

(a) ASM *vs.* FSM

(b) Noise Margin.